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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application Serial No
Filing Date August 31, 2000
nventor Keiji Jono et al.
AssigneeKMT Semiconductor, LTD
Group Art Unit
Examiner
Attorney's Docket No KM1-001
Fitle: Methods of Forming an Isolation Trench in a Semiconductor, Methods of
Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods of
Forming an Isolation Trench-Isolated Transistor, Trench-Isolated Transistor,
Trench Isolation Structures Formed in a Semiconductor, Memory Cells and
DRAMS

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - See Attached Form PTO-1449

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: 3-10-03

D. Brent Kenady

Reg. No. 40,045

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. KM1-001

SERIAL NO. 09/652,550

LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)

APPLICANT: Keiji Jono et al.

FILING DATE

GROUP

			U.	S. PATENT DOCUMENTS				
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filin If App	g Date ropriate
	AA	6,034,409	03/07/2000	Sakai et al.				
	AB 6,171,924 B1		01/09/2001	Wang et al.				
	AC	6,154,417	11/28/2000	Kim				
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		OTHER RE	FERENCES (i	ncluding Author, Title, Date, Perti	nent Pages, Etc.)	2	
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conformance and not considered. Include copy of this form with next communication to applicant.